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McDERMOTT, WILL & EMERY
600 13th Street, N.W.
Washington, DC 20005-3096

EXAMINER	
O'BRIEN, BARRY J	

ART UNIT	PAPER NUMBER
2183	4

DATE MAILED: 12/15/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/756,863	YOSHIDA, TOYOHIKO	
	Examiner	Art Unit	
	Barry J. O'Brien	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 January 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 2.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

1. Claims 1-19 have been examined.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed on record in the file: IDS as received on 1/10/2001 and Priority Papers as received on 1/10/2001.

Specification

3. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Objections

4. Claim 18 is objected to because of the following informalities:

   a. Claim 18 is said to dependent on claim 15. This is incorrect antecedent basis for the claim, which should depend on either claim 16 or 17. Please correct the claim to have a valid parent claim. For the purposes of this examination, it will be assumed that claim 18 is dependent on claim 17.

5. Appropriate correction is required.

Claim Rejections - 35 USC § 112

6. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

7. Claim 18 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Claim 18 recites the limitation, "wherein the wait number of said bus when an instruction read out from said instruction memory with a translator is transferred to said processor is controlled to be larger than the wait number of said bus when an instruction read out from said second instruction memory is transferred to said processor." The Applicant's specification does not disclose what a "wait number" is defined as, nor does it discuss how the "wait numbers" of reading an instruction out of the different memories differ. Therefore, one of ordinary skill in the art would not have been able to make and/or use the invention as claimed in claim 18.

8. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

9. Claims 3, 13, 15 and 18 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

10. Claim 3 recites the limitation "having a length larger than the instruction length." It is unclear which instruction of which instruction architecture this is in reference to, as well as how this limitation affects the translation that is dependent upon it. For the purposes of this examination, it will be assumed that the translated instructions have a larger total length than the

original instruction in the first instruction architecture. Please correct to more distinctly claim and further clarify the claim language.

11. Claim 13 recites the limitations "the processing to translate" as well as "the processing of outputting." It is unclear what this language means, as it is not grammatically correct English. Furthermore, the claim recites the limitation "includes a selector to select one of the processing." It is unclear how a selector can select between two "processings." Please correct the claim language to more clearly point out what the applicant is claiming.

12. Claim 15 recites the limitation "an instruction output by said translator and the corresponding instruction in said first instruction architecture held in said instruction cache" on the last 2 lines of the claim. It is unclear how this limitation relates to the language of the claim. It does not appear to be a determining factor in determining "whether or not an instruction corresponding to the instruction to the address is held in said instruction cache", nor does it appear to affect the selector. Please correct the claim language to more clearly point out how this limitation relates the rest of the claim.

13. Claim 18 recites the limitation "wait number" in second and fourth lines of the claim. There is insufficient antecedent basis for this limitation in the claim. Please correct the claim language to more clearly point out what this language is in reference to. For the purposes of this examination, it is assumed that "wait number" refers to the time it takes to read out from the two instruction memories.

14. The claims are generally narrative and indefinite, failing to conform with current U.S. practice. They appear to be a literal translation into English from a foreign document and are replete with grammatical and idiomatic errors.

Claim Rejections - 35 USC § 102

15. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

16. Claims 1 and 12-18 are rejected under 35 U.S.C. 102(b) as being anticipated by Emma, U.S. Patent No. 5,619,665.

17. Regarding claim 1, Emma has taught in a processor (608 of Fig.6) operating with instructions in a first instruction architecture as a native instruction, an instruction translator used with an instruction memory to store an instruction in a second instruction architecture different from said first instruction architecture, for translating an instruction in said second instruction architecture into an instruction in said first instruction architecture for application to said processor (see Col.3 lines 2-17), said instruction translator comprising:

a. A translator (606 of Fig.6) for reading out an instruction from said instruction memory (602 of Fig.6) in response to a received first address in said instruction memory of an instruction to be executed by said processor and translating the read out instruction in said second instruction architecture into an instruction in said first instruction architecture (see Col.12 lines 42-56),

b. An instruction cache (604 of Fig.6) for temporarily holding the instruction in said first instruction architecture after the translation by said translator in association with the first address in said instruction memory (see Col.12 lines 51-56),

c. A selector for searching said instruction cache in response to a received second address of an instruction to be executed by said processor, and for selectively outputting, based on a determination result of whether or not an instruction corresponding to the instruction of the second address is held in said instruction cache, an instruction output by said translator and the corresponding instruction held in said instruction cache (see Col.12 lines 59-67 and Col.13 lines 1-6).

18. Regarding claim 12, Emma has taught an instruction memory attached with a translator, used with a processor operating with an instruction in a first instruction architecture as a native instruction (see Col.3 lines 2-17), comprising:

a. An instruction storage unit (602 of Fig.6) to store an instruction in a second instruction architecture (see Col.12 lines 42-49),

b. An instruction translator (606 of Fig.6) to translate an instruction in said second instruction architecture output from said instruction storage unit into an instruction in said first instruction architecture for application to said processor (see Col.12 lines 42-56).

19. Regarding claim 13, Emma has taught the instruction memory attached with a translator according to claim 12, wherein said instruction translator includes a selector to select one of the processing to translate the instruction in said second instruction architecture into the instruction in said first instruction architecture and the processing of outputting the instruction in said second instruction architecture as it is, based on an address of an instruction to be executed which is read out from said instruction storage unit (see Col.12 lines 59-67 and Col.13 lines 1-6).

20. Regarding claim 14, Emma has taught the instruction memory attached with a translator according to claim 12, further comprising an address translator to translate an address at the time of reading from said instruction storage unit (see Col.11 lines 4-13). Here, Emma has taught the address of source instructions A, B, and C being translated to a native instruction X_1 having the address of source instruction A, the translating the addresses of B and C to be the address of A (X_1).

21. Regarding claim 15, Emma has taught the instruction memory attached with a translator according to claim 12, wherein said instruction translator includes:

a. A translator (606 of Fig.6) to read out the instructions in said second instruction architecture from said instruction storage unit in response to a received first address of an instruction to be execute by said processor and translate the read out instruction in said second instruction architecture into the instruction in said first instruction architecture (see Col.12 lines 42-56),

b. An instruction cache (604 of Fig.6) to temporarily hold the instruction in said first instruction architecture after the translation by said translator in association with the first address (see Col.12 lines 51-56),

c. A selector to search said instruction cache in response to a received second address of an instruction to be executed by said processor and selectively output to said processor, based on a determination result of whether or not an instruction corresponding to the instruction of the address is held in said instruction cache, an instruction output by said translator and the corresponding instruction in said first

instruction architecture held in said instruction cache (see Col.12 lines 59-67 and Col.13 lines 1-6).

22. Regarding claim 16, Emma has taught a data processing apparatus, comprising:

a. A processor operating (608 of Fig.6) with an instruction in a first instruction architecture as a native instruction (see Col.3 lines 2-17),

b. A bus (612 of Fig.6) to which said processor is connected,

c. An instruction memory (602 of Fig.6) with a translator (606 of Fig.6) interconnected with said processor through said bus,

d. Said instruction memory with a translator including:

i. An instruction storage unit (602 of Fig.6) to store an instruction in said second instruction architecture transferred from said processor through said bus (see Col.12 lines 42-49),

ii. An instruction translator to translate the instruction in said second instruction architecture output from said instruction storage unit into an instruction in said first instruction architecture for application to said processor through said bus (see Col.12 lines 42-56).

23. Regarding claim 17, Emma has taught the data processing apparatus according to claim 16, further comprising:

a. A second instruction memory (604 of Fig.6) interconnected to said processor through said bus, said second instruction memory including:

i. An instruction storage unit (604 of Fig.6) to store an instruction in said first instruction architecture transferred from said processor through said bus (see Col.12 lines 51-56),

ii. An instruction reading circuit responsive to an address signal applied from said processor through said bus for applying an instruction in said first instruction architecture output from said instruction storage unit to said processor through said bus (see Col.12 lines 59-67 and Col.13 lines 1-6).

24. Regarding claim 18, Emma has taught the data processing apparatus according to claim 17, wherein the wait number of said bus when an instruction read out from said instruction memory with a translator is transferred to said processor is controlled to be larger than the wait number of said bus when an instruction read out from said second instruction memory is transferred to said processor (see Col.12 lines 59-67 and Col.13 lines 1-6).

25. Here, as mentioned above, it is assumed that the wait number of a bus is the amount of time that it takes to read out from each memory. Because when an instruction is read out of the first instruction memory, it needs to be translated, while when reading out of the second instruction memory the instruction has already been translated (see Col.12 lines 65-67 and Col.13 lines 1-6), it is inherent that it will take less time to read out from an instruction memory that does not have to perform a translation.

Claim Rejections - 35 USC § 103

26. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

27. Claims 2-3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Emma, U.S. Patent No. 5,619,665 as applied to claim 1 above, and further in view of Dickol et al., U.S. Patent No. 5,875,336.

28. Regarding claim 2, Emma has taught the instruction translator according to claim 1, but has not explicitly taught wherein said second instruction architecture is a variable length instruction architecture, and said translator includes a variable length translator for translating an instruction in said second instruction architecture read out from said instruction memory into one or more instruction in said first instruction architecture, the number of which depends on an instruction length of the read out instruction in said second instruction architecture.

29. However, Dickol has taught a variable length instruction architecture being translated in real time into one or more instructions of a second instruction architecture based on the varying lengths of instructions in the variable length instruction architecture (see Col.3 lines 29-38 and Col.4 lines 13-14, 21-27) in order to improve performance when executing non-native instructions on more common native-instruction-based hardware (see Col.1 lines 47-61 and Col.2 lines 15-18). One of ordinary skill in the art would have recognized that a priority of microprocessor designers is to improve performance while minimizing cost and hardware complexity. Therefore, one of ordinary skill in the art at the time of the invention would have found it obvious to modify Emma to further decode instructions from a non-native variable length instruction set into one or more native instructions in order to improve processor

performance when executing non-native instructions while minimizing the additional hardware required to do so.

30. Regarding claim 3, Emma in view of Dickol has taught the instruction translator according to claim 2, wherein said variable length translator translates the instruction in said second instruction architecture read out from said instruction memory into an instruction in said first instruction architecture depending on the instruction length of said read out instruction in said second instruction architecture and having a length larger than the instruction length (see Col.3 lines 29-38 and Col.4 lines 13-14, 21-27). As noted above, here it is assumed that the translated second instruction architecture instructions will have a total length larger than the original first instruction architecture instruction (see Figs. 3-5).

31. Claims 4 and 6-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Emma, U.S. Patent No. 5,619,665 in view of Dickol et al., U.S. Patent No. 5,875,336 as applied to claims 1-3 above, and further in view of Goettelmann et al., U.S. Patent No. 5,313,614.

32. Regarding claim 4, Emma in view of Dickol have taught the instruction translator according to claim 3, but have not explicitly taught wherein each instruction in said first instruction architecture includes one or a plurality of sub instructions, and the number of the sub instructions included in the instruction in the first instruction architecture translated by said variable length translator depends on the instruction length of said read out instruction in said second instruction architecture.

33. However, Goettelmann has taught the translation from a source instruction architecture (see "source machine code" of Fig.11) into a native instruction architecture (see "translated code" of Fig.11), wherein the native architecture contains a plurality of sub-instructions (see

"expanded intermediate language code" of Fig.11), sub-instructions which can then be removed if necessary in order to reduce the translated code size (see Col.4 lines 6-18). One of ordinary skill in the art would have recognized that it is desirable to reduce the size of instruction code so that less hardware (memory space) is needed, thus lowering costs. Therefore, one of ordinary skill in the art would have found it obvious to modify the instruction translator of Emma in view of Dickol to further translate instructions from a source architecture into a native architecture that includes a plurality of sub-instructions in order to reduce the amount of instruction storage required to store the translated code. Furthermore, because the number of native instructions are dependent on the length of the varying-length source instruction as shown above, and because the number of sub instructions depend on the native instructions, then the number of sub-instructions depend on the length of the source instructions.

34. Regarding claim 6, Emma in view of Dickol has taught the instruction translator according to claim 1, but have not explicitly taught wherein:

a. Each instruction in said first instruction architecture can include one or a plurality of sub instructions,

b. Said translator translates a plurality of instructions in said second instruction architecture read out from said instruction memory into an instruction in said first instruction architecture including sub instructions, the number of which depends on the number of said plurality of instructions.

35. However, However, Goettelmann has taught the translation from a source instruction architecture (see "source machine code" of Fig.11) into a native instruction architecture (see "translated code" of Fig.11), wherein the native architecture contains a plurality of sub-

instructions (see "expanded intermediate language code" of Fig.11), sub-instructions which can then be removed if necessary in order to reduce the translated code size (see Col.4 lines 6-18). One of ordinary skill in the art would have recognized that it is desirable to reduce the size of instruction code so that less hardware (memory space) is needed, thus lowering costs. Therefore, one of ordinary skill in the art would have found it obvious to modify the instruction translator of Emma in view of Dickol to further translate instructions from a source architecture into a native architecture that includes a plurality of sub-instructions in order to reduce the amount of instruction storage required to store the translated code. Furthermore, because the number of native instructions are dependent on the length of the varying-length source instruction as shown above, and because the number of sub instructions depend on the native instructions, then the number of sub-instructions depend on the length of the source instructions.

36. Regarding claim 7, Emma in view of Dickol in further view of Goettelmann have taught the instruction translator according to claim 6, wherein the number of sub instructions included in the instruction in said first instruction architecture after said translation is equal to the number of said plurality of instructions (see "BEQ Label instruction" of "source machine code", its corresponding "BFALSE FlagZ, Label" instruction of "translated code", with associated sub-instruction "BFALS.d FlagZ, Label" of "expanded intermediate language code", all of Fig.11 of Goettelmann).

37. Claims 8 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Emma, U.S. Patent No. 5,619,665 in view of Gregor, U.S. Patent No. 5,023, 776.

38. Regarding claim 8, Emma has taught the instruction translator according to claim 1 as shown above, wherein:

a. Said translator translates said read out instruction in said second instruction architecture into one or a plurality of instructions as the instruction in said first instruction architecture (see Col.12 lines 42-56)

39. Emma has not explicitly taught where said instruction translator further comprises a controller for controlling said instruction cache so that said instruction cache holds each of said one or said plurality of instruction held in said instruction cache as an entry which can be invalidated in one of first and second conditions.

40. However, Gregor has taught the holding of a cache line within a cache so that it cannot be replaced until an EOP signal is detected in order to reduce cache busy time and improve processor performance (see Col.22 lines 36-67). One of ordinary skill in the art would have recognized that it is desirable, as well as a main goal of microprocessor design, to improve the performance of a microprocessor. Therefore, one of ordinary skill in the art would have found it obvious to modify the cache of Emma to hold a plurality of instructions in a cache until an EOP signal is detected. Furthermore, because the claim language is in the alternative format, only one of the two invalidation condition requirements is required to be met, and thus the EOP signal that is detected (see Col.22 lines 56-57 of Gregor) can be considered such a signal.

41. Regarding claim 10, Emma in view of Gregor has taught the instruction translator according to claim 8, wherein said controller outputs a signal asserted when a new instruction cannot be held in said instruction cache without invalidating an entry which can be invalidated in the second condition (see Col.22 lines 36-67).

42. Claims 9 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Emma, U.S. Patent No. 5,619,665 in view of Gregor, U.S. Patent No. 5,023, 776, in further view of Schacham et al., U.K. Patent Application GB220481A.

43. Regarding claim 9, Emma in view of Gregor have taught the instruction translator according to claim 8, wherein:

a. Said first condition is a holding control condition by hardware control based on a prescribed algorithm by said instruction cache (see Col.22 lines 36-67).

44. Emma in view of Gregor has not explicitly taught wherein the said second condition is a condition in which an explicit invalidation instruction is applied from the outside of said instruction cache.

45. However, in the parent claim of claim 9 only one of the two invalidation conditions must be met. Therefore, because Emma in view of Gregor has satisfied one of the conditions, namely the holding control condition as shown above, the claim language is satisfied.

46. Furthermore, even though the alternative form claim language is met, Schacham has taught that a cache invalidation instruction can be executed to invalidate the entire instruction cache or a portion of it (see p.4 lines 28-30) in order to maintain proper cache coherence and provide better processor performance (see p.2 lines 8-23). One of ordinary skill in the art would have recognized that it is desirable, as well as a main goal of microprocessor design, to improve the performance of a microprocessor. Therefore, one of ordinary skill in the art would have found it obvious to modify the instruction cache of Emma in view of Gregor to allow a cache invalidation instruction to be executed so that cache coherency is maintained and processor performance is improved.

47. Regarding claim 11, Emma in view of Gregor has taught the instruction translator according to claim 8, wherein said translator translates the read out instruction in said second instruction architecture into the plurality of instructions as the instruction in said first instruction architecture (see Col.12 lines 42-56), but has not explicitly taught where said controller provides said first condition with one of said plurality of instructions and said second condition with each of said plurality of instructions but said one instruction.

48. However, Schacham has taught that a cache invalidation instruction can be executed to invalidate the entire instruction cache or a portion of it (see p.4 lines 28-30) in order to maintain proper cache coherence and provide better processor performance (see p.2 lines 8-23). One of ordinary skill in the art would have recognized that it is desirable, as well as a main goal of microprocessor design, to improve the performance of a microprocessor. Therefore, one of ordinary skill in the art would have found it obvious to modify the instruction cache of Emma in view of Gregor to allow a cache invalidation instruction to be executed so that cache coherency is maintained and processor performance is improved.

49. Emma in view of Gregor in view of Schacham has taught the invalidation of instructions in a cache based upon one of two conditions, namely a holding control condition as taught by Gregor, and a cache invalidation instruction as taught by Schacham. One of ordinary skill in the art would have recognized that because some instructions will have the first condition associated with them, and others will have the second condition associated with them. Therefore, one of ordinary skill in the art would have found it obvious that the processor of Emma in view of Gregor in view of Schacham will provide one instruction with a first condition, and other instructions with a second condition.

50. Claims 5 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Emma, U.S. Patent No. 5,619,665, as applied to claims 1 and 18 above.

51. Regarding claim 5, Emma has taught the instruction translator according to claim 1, wherein said translator includes a plurality of translators which translate a plurality of instruction in said second instruction architecture read out from said instruction memory into one instruction in said first instruction architecture (see Col.3 lines 2-17). While a plurality of translators is not explicitly taught, the translation of a plurality of instructions in the second instruction architecture into one instruction in the first instruction architecture is taught. The inclusion of a plurality of translators to perform the same function as a single translator provides no new or unexpected result over the prior art. Therefore, one of ordinary skill in the art would have found it obvious to duplicate the translator, creating a plurality of translators for translating instructions in a second instruction architecture into a single instruction in a first instruction architecture (see In re Harza, 274 F.2d 669, 671, 124 USPQ 378, 380 (CCPA 1960)).

52. Regarding claim 19, Emma has taught the data processing apparatus according to claim 18, further comprising a second instruction memory (604 of Fig.6) with a translator interconnected to said processor through said bus, said second instruction memory with a translator including:

a. An instruction storage unit (604 of Fig.6) to store an instruction in a second instruction architecture different from said second instruction architecture, said instruction in said third instruction architecture being transferred from said processor through said bus (see Col.12 lines 51-56),

b. An instruction translation circuit responsive to an address signal applied from said processor through said bus, for translating an instruction in said third instruction architecture output from said instruction storage into an instruction in said first instruction architecture for application to said processor (see Col.12 lines 59-67 and Col.13 lines 1-6).

53. Emma has not explicitly taught a third instruction memory with a translator for translating a third instruction architecture into a first instruction architecture is not explicitly taught.

54. However, adding a third instruction memory and corresponding third instruction architecture provides no new or unexpected result over the prior art except for allowing the additional translation of a third instruction architecture. But this could be achieved simply by replacing the second instruction architecture with the third architecture, as there are no claim limitations that require the two instruction architectures to be translated simultaneously. Therefore, one of ordinary skill in the art would have found it obvious to duplicate the hardware used to operate on a second instruction architecture as taught by Emma in order to operate on a third instruction architecture (see In re Harza, 274 F.2d 669, 671, 124 USPQ 378, 380 (CCPA 1960)).

Conclusion

55. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Applicant is reminded that in amending in response to a rejection of claims, the patentable novelty must be clearly shown in view of the state of the art disclosed by the

references cited and the objections made. Applicant must also show how the amendments avoid such references and objections. See 37 CFR § 1.111(c).

56. Carbine et al., U.S. Patent No. 5,630,083, has taught a decoder which can decode an instruction into multiple micro-instructions.

57. Robinson et al., U.S. Patent No. 5,307,504, has taught a method for translating a CISC instruction into multiple RISC instructions.

58. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Barry J. O'Brien whose telephone number is (703) 305-5864. The examiner can normally be reached on Mon.-Fri. 7am-4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (703) 305-9712. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

Barry J. O'Brien
Examiner
Art Unit 2183

RICHARD L. ELLIS
PRIMARY EXAMINER

BJO
12/11/2003